REMARKS/ARGUMENTS

Applicants wish to thank the Examiner for taking the time to conduct an interview with the Applicants' attorney. Claims 1, 4-19, 22-32, and 35-43 remain pending. Claims 22 and 35 have been amended, as recited hereinabove.

Claims 22 and 35 have been rejected, under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is believed that claims 22 and 35, as amended, are now in proper form. This rejection is now rendered moot.

Claims 1, 4, 6-14, 18-19, 22-32 and 35-43 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Grieff et al. (US Patent No. 6,961,813) (hereinafter "Grieff") in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" (hereinafter "SATA vs. PATA") and Utsunomiya et al. (US Publication No. 2003/0131166) (hereinafter referred to as "Utsunomiya"). It is believed that the foregoing claims, as recited hereinabove are patentable and all claims depending therefrom are patentable over Grieff in view SATA vs. PATA and of Utsunomiya. As a separate basis of patentability, the combination of Grieff and Utsunomiya, as the basis of rejection, is disagreed therewith because neither reference suggests or hints at the teachings of the other and are believed to be non-analogous art.

Claim 5 is rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff, SATA vs. PATA and Utsunomiya, as applied to claims 1,4,6-14 and 18-43, and further in view of Boucher et al. (US Patent 6,434,620) (hereinafter "Boucher")

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff in view of SATA vs. PATA, Utsunomiya, and "Serial ATA Specification" (hereinafter Serial ATA Specification).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff in view of SATA vs. PATA, and Shin et al. (US Patent 7,154,905) (hereinafter "Shin").

The combination of Utsunomiya and Greiff are not believed to render the claimed invention obvious and therefore unpatentable. The combination does not disclose "an arbitration and control circuit, …, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state" because, among other reasons, Grieff's host ports are state machines and not any

type of storage devices and Utsunomiya does not have a switch. Thus, the combination cannot perform the concurrent access to the device by the host of the claimed invention. There is no disclosure regarding task files or any type of storage queuing device being placed prior to the switch in Grieff. Utsunomiya certainly does not suggest anything of the like.

Additionally, the combination simply will not work in a manner consistent with "selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state". The host ports of Grieff 130 and 132 are Link Layer ports, the task file (which is at the application layer) queue of Utsunomiya can not be placed in host ports 130 and 132 of Grieff Thus, it is believed that the combination forming the basis of the foregoing rejections are not operational relative to the claimed invention and therefore do not render the claimed invention obvious.

As a separate basis of patentability, combining Utsunomiya and Grief are believed to be wrong because the latter discloses a system using the serial ATA (SATA) standard and the former discloses a system using the ATA standard and there is no suggestion of one as to standard of the other. These two standards are very different, as discussed during the Interview. Among their differences are: SATA uses a serial link that uses Gigabit technology and 8b/10b encoding for connectivity whereas ATA uses a parallel bus; and The architecture of SATA is based on four layers of communication: Application, Transport, Link, and Phy whereas only one layer (Application) of communication is used in ATA. To combine the foregoing standards would be to re-design the systems. The claimed invention is directed to a system using the SATA standard, which is not disclosed by Utsunomiya.

Regarding claim 4, the combination does not include "a device task file".

Therefore, all independent claims 1, 20 and 33, are non-obvious and patentable over Grieff in combination with Utsunomiya. It is therefore also believed that all claims depending therefrom are patentable. Moreover, as all other rejections appear to combine Grieff and Utsunomiya, they are also believed to be moot in light of the foregoing arguments/remarks.

Reconsideration and allowance of claims 1, 4-19, 22-32, and 35-43 is hereby respectfully requested. Applicants submit that the subject application is now in condition

for allowance and an early notice thereof is respectfully requested. Should any further amendment be required prior to passing the application to issue, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Respectfully submitted,
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